Synchronization Architecture in Parallel Programming Models

PhD Thesis

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Outline

Introduction

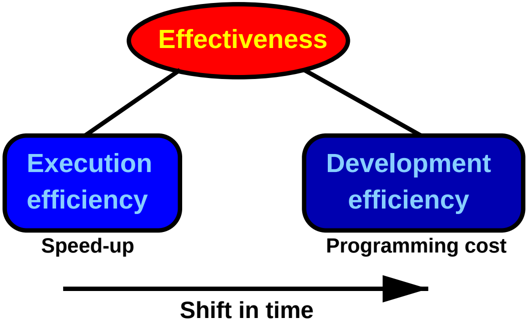
Conceptual approach and models review

Theoretical and algorithmic approach

Experimental approach

Conclusion

Motivation



[Siegel2000] [Smith2001] [Danelutto2003]

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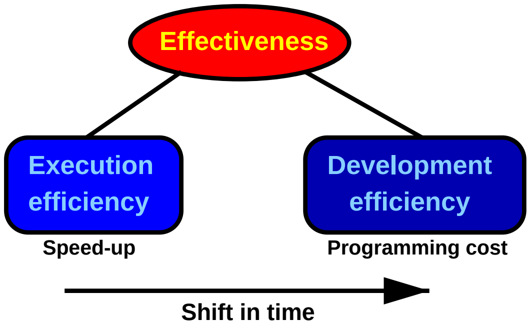

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- No well-established parallel computing model or reference architecture

  [SkillicornTalia98]

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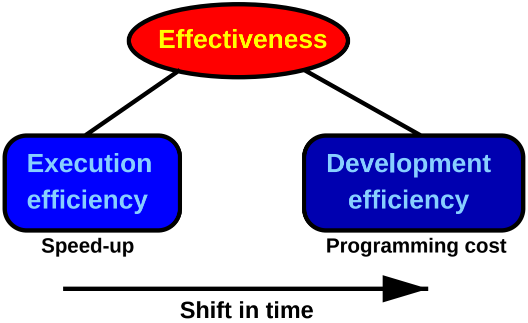

[Siegel2000] [Smith2001] [Danelutto2003]

- No well-established parallel computing model or reference architecture [SkillicornTalia98]
- Lack of a *Parallel Programming Model (PPM)* which achieves both:
  - Software development capabilities
  - Portability and efficient implementations

Parallel systems modeling challenges

Existing approaches

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- High abstract level
  - + Elegant semantic models
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  - – Reduce the expressive power
  - \+ Simple & analyzable structures

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The expressive power and analyzability of a model appear to be highly related to communication/synchronization

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    [GelernterCarriero92]
  - Synchronization distinguishes parallel from sequential solutions

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  We present systematic transformation methods to map non-SP applications into SP form

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  We show that one SA class, called SP, groups the most interesting models

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  We present systematic transformation methods to map non-SP applications into SP form

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We will show that SP PPMs bring a good trade-off between expressive power and analyzability, being a good choice for general-purpose parallel computing

Approach

Three-step approach

Introduction

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- Conceptual
  - SA classification
  - Review of models at different abstraction levels
  - Relate SA to PPM characteristics
  - Detect which applications naturally map to each class

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  - SP graph characterization
  - NSP to SP transformation (algorithmic) techniques
  - Potential performance loss study

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- Experimental
  - Graph modeling of applications
  - Experiments with synthetic graphs
  - Experiments with real application graphs

SA classification criteria

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- Classes:
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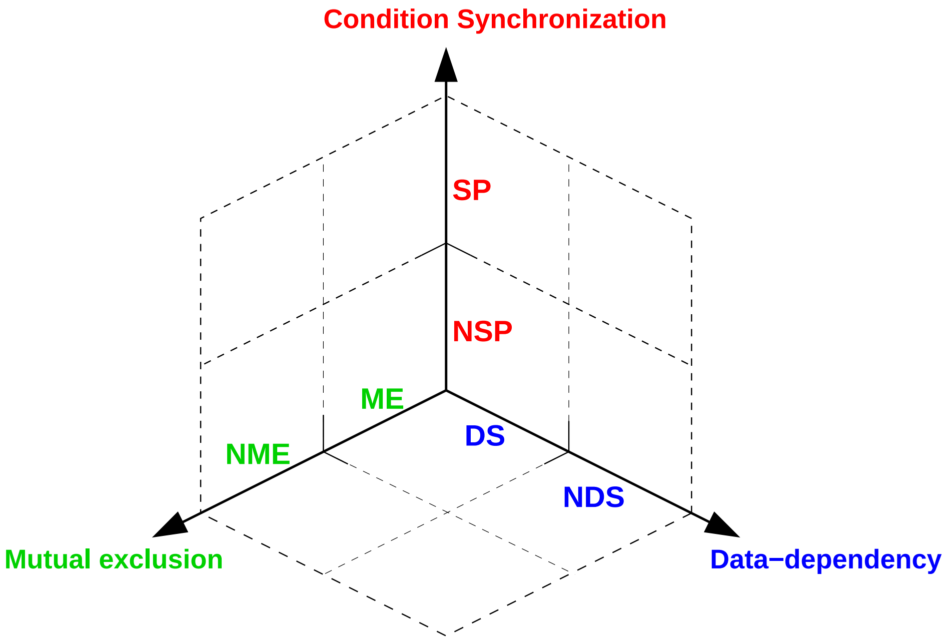
  - CS axis: SP (nested-parallelism, cobegin-coend) vs. NSP
- Data-dependent or dynamic structures (DS)
  - Dynamic conditions and data-dependent synchronizations
  - Impact on analyzability properties [SkillicornTalia98]
  - DS axis: DS vs. NDS

SA classification



Conceptual

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		SP	NSP
ME	DS	(SP,ME,DS)	(NSP,ME,DS)
ME	NDS	(SP,ME,NDS)	(NSP,ME,NDS)
NME	DS	(SP,NME,DS)	(NSP,NME,DS)
NME	NDS	(SP,NME,NDS)	(NSP,NME,NDS)

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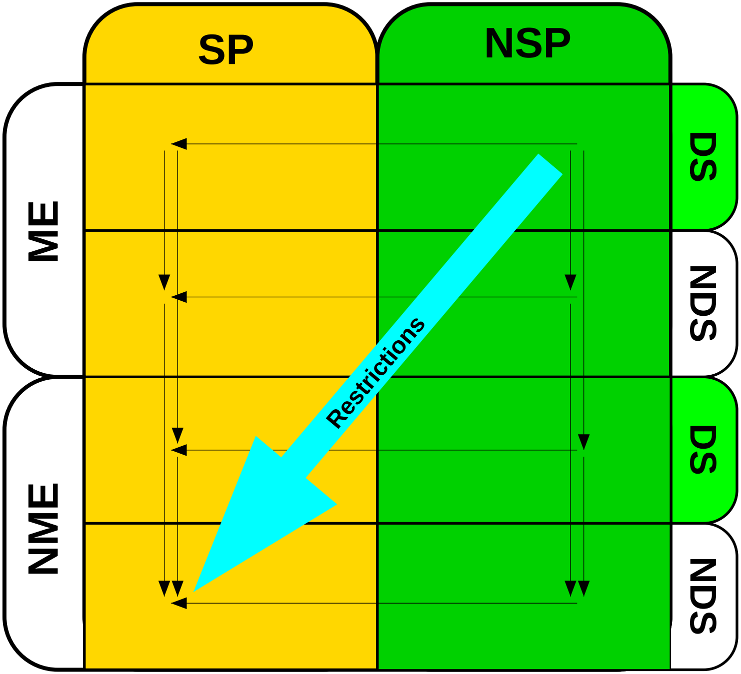

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- Quantitative study of performance is possible [JuurlinkWijshof98]

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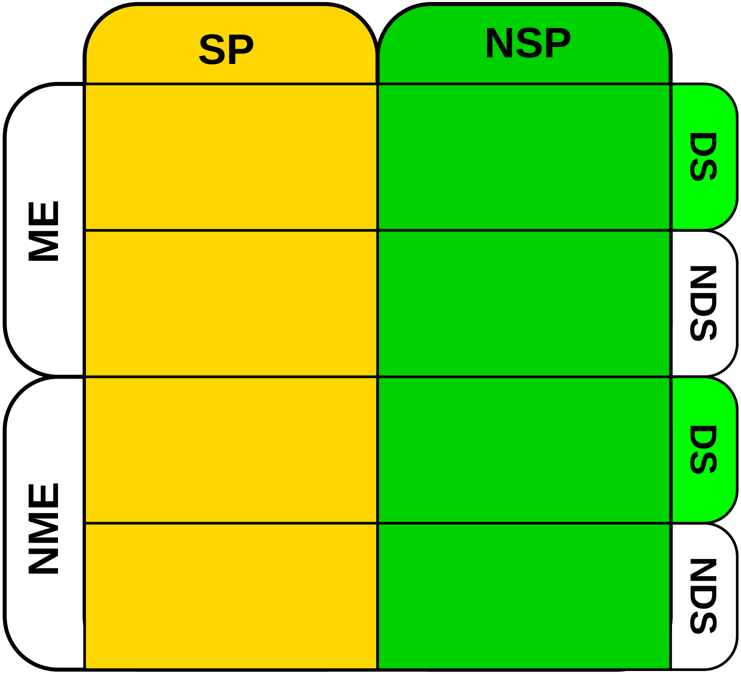
- In this work:
  - Review of models to determine adequacy and relate it to SA
  - For the most relevant SA classes, comparative performance study

Classification discussion



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NME	DS	Cilk	
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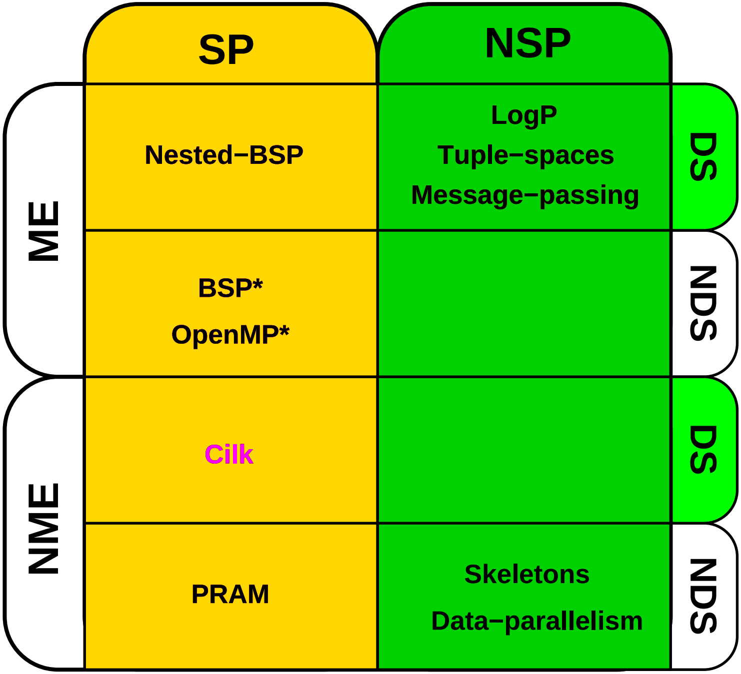

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Cellular-Automata computation

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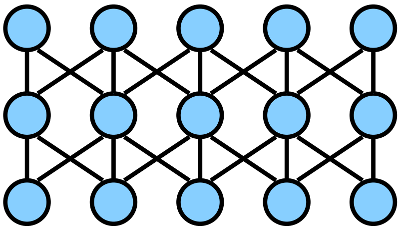

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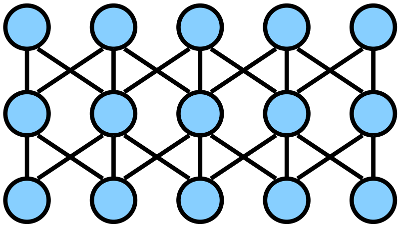

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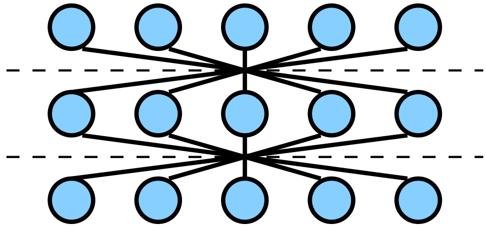

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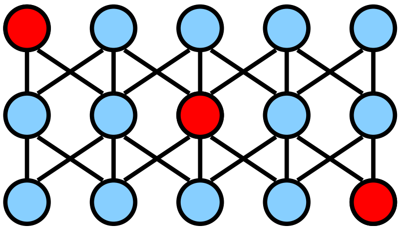

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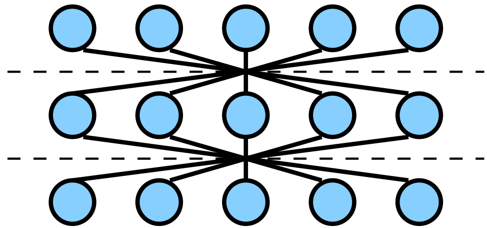

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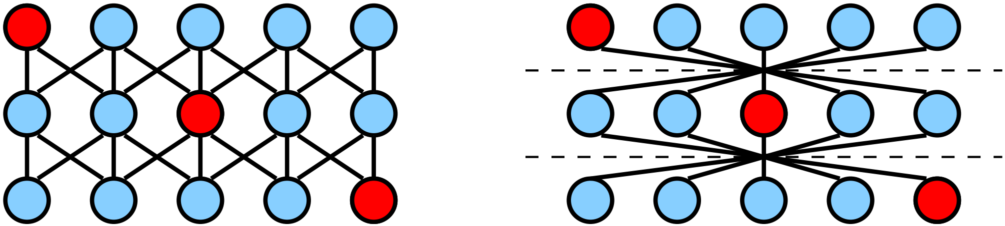

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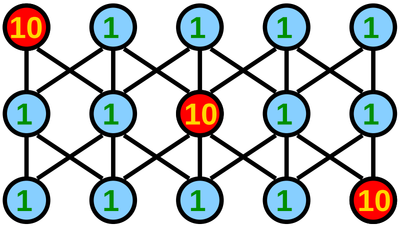

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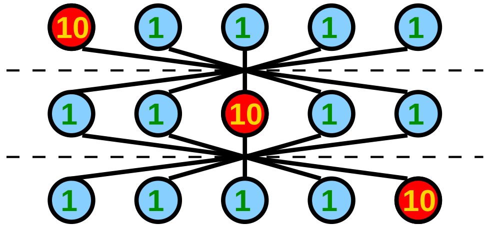

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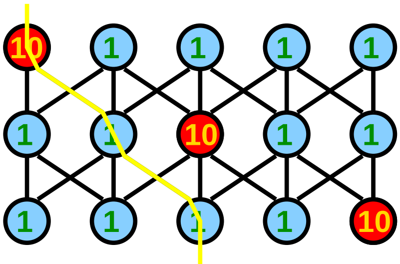

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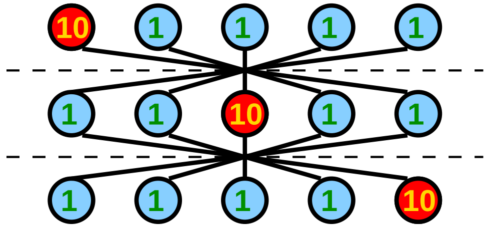

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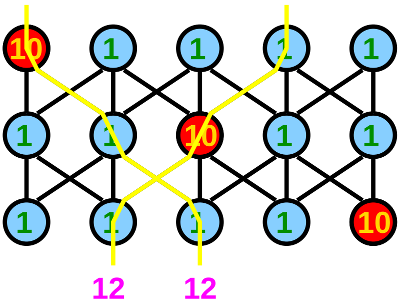

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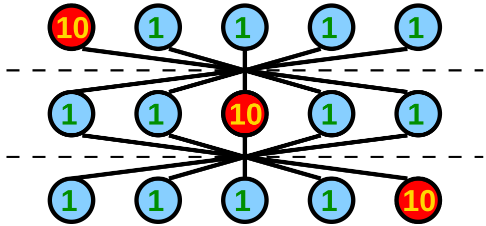

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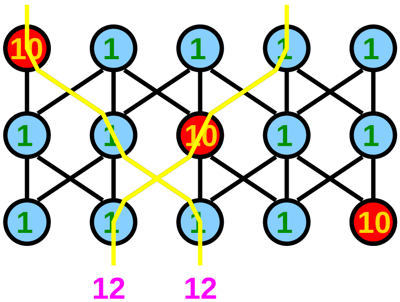

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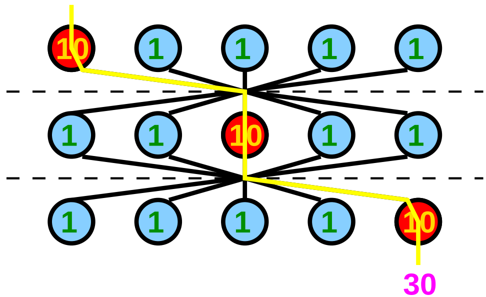

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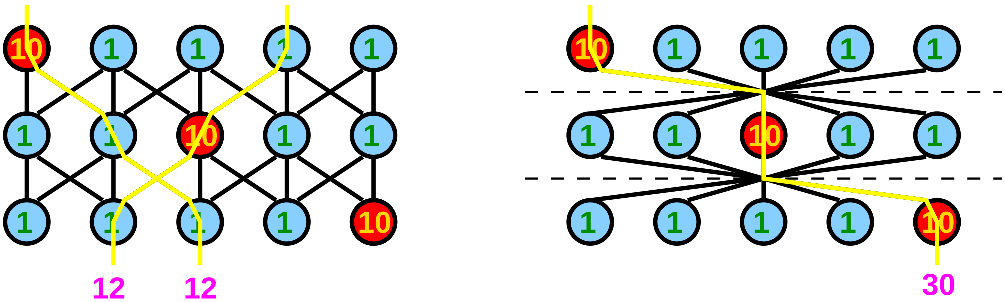

NSP version **SP version**

It is necessary to study the transformations: NSP $\longrightarrow$ SP
and their potential performance impact

Theoretical approach

Theoretical

Graphs

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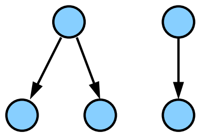

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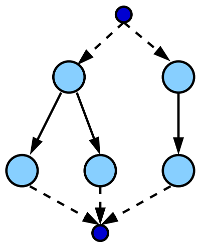

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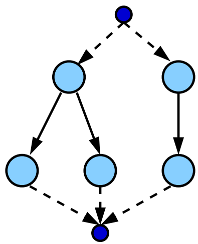

- Modelization of a parallel computation structures with a graph:
  - AoN (Activity on Nodes)
  - Edges: Condition synchronization (execution order)

SP graph

- Compositional recursive definition: [Valdes.et al92]

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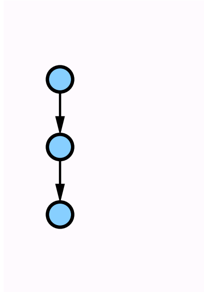

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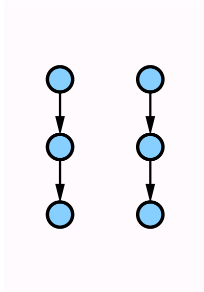

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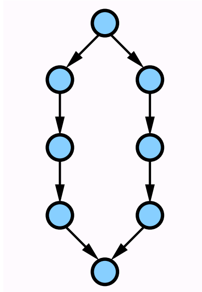

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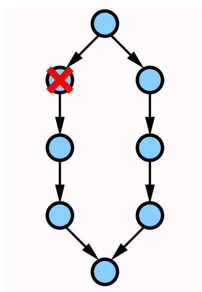

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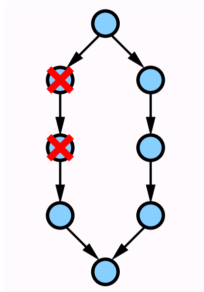

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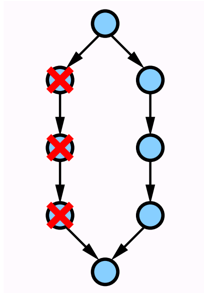

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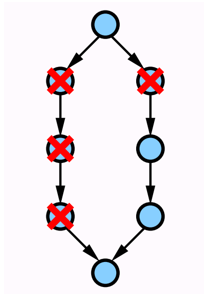

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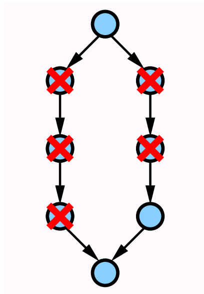

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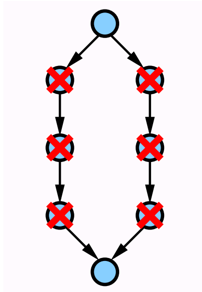

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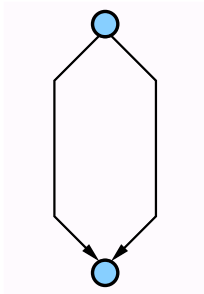

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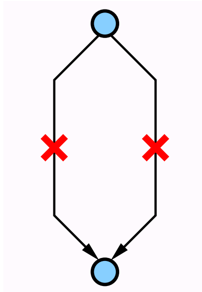

Theoretical

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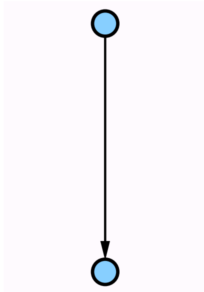

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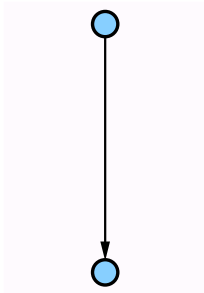

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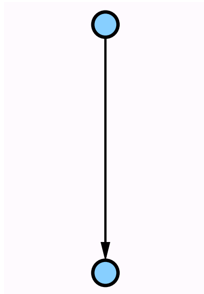

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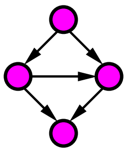

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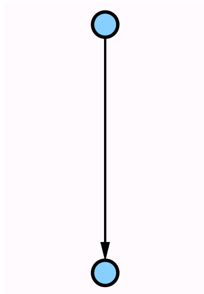

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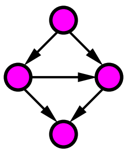

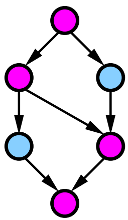

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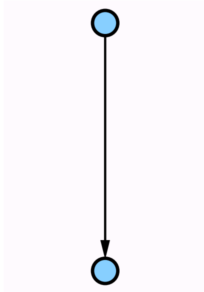

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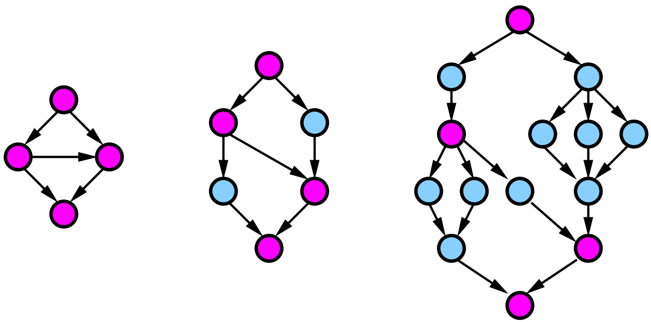

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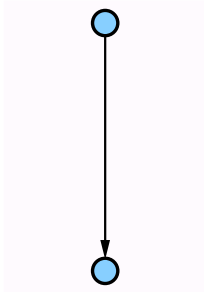

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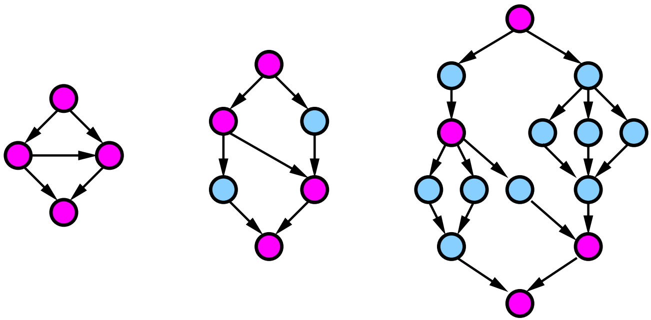
- NSP: Combinations of forbidden subgraphs [Dissertation 3.3.3]



Transformation strategies - I

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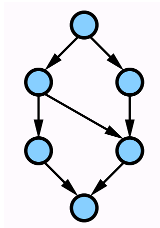

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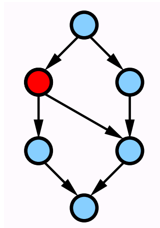

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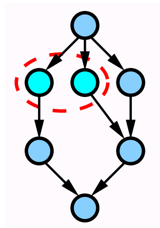

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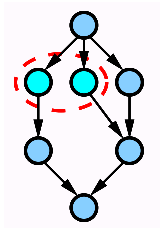

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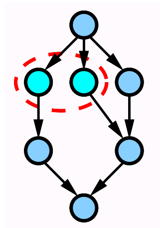

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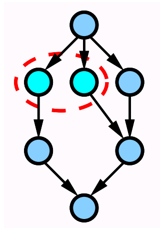

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  - Not appropriate for general purposes

Transformation strategies - II

- Added dependencies

Theoretical

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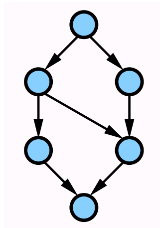

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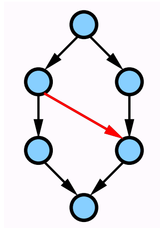

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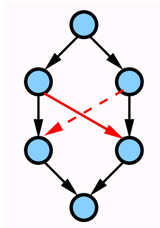

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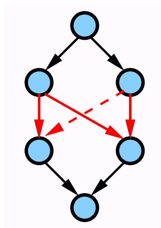

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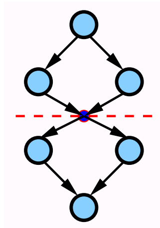

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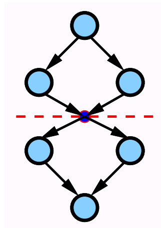

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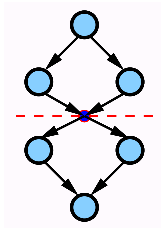

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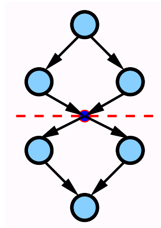

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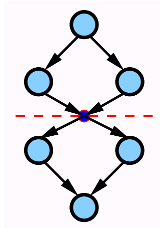

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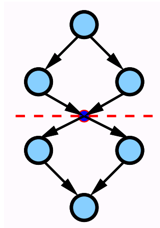

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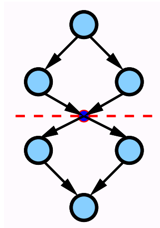

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- We focus on SP-izations

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- Well-known system [Malony.et al94] associated to the bulk-synchronous concept

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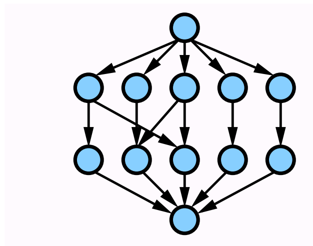

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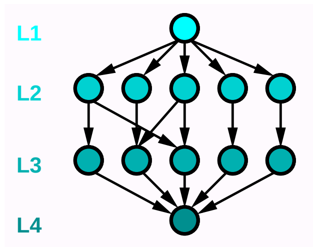

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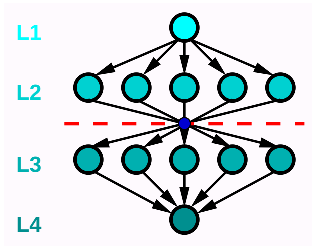

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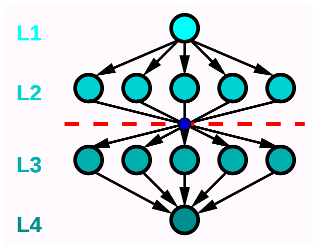

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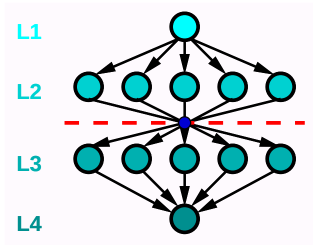

- Low complexity bounds: $O(m + n)$

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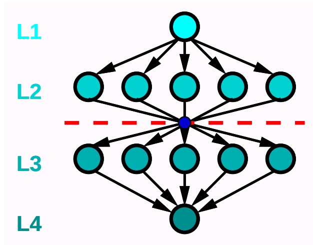

- Low complexity bounds: $O(m+n)$
- It does not exploit SP graphs or possibility of local resynchronizations

Algorithm 1

- Local problems solving + Keep SP subgraphs untouched

Theoretical

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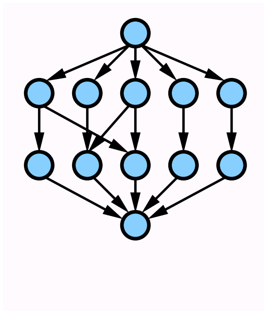

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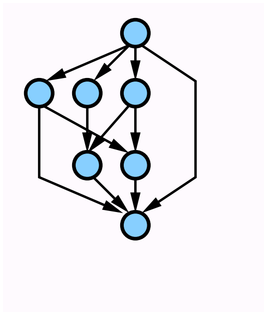

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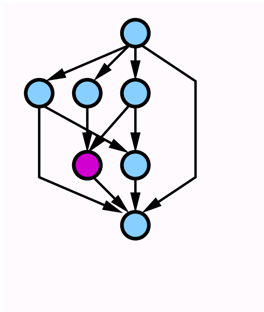

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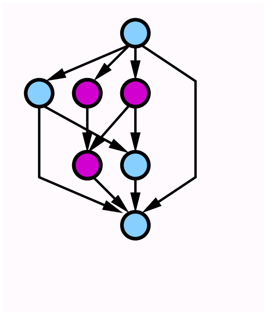

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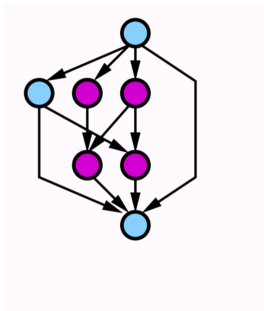

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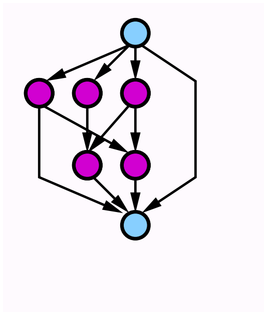

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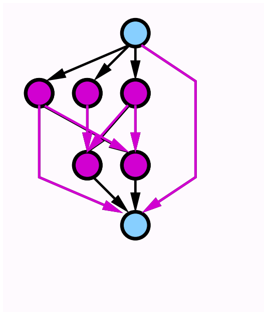

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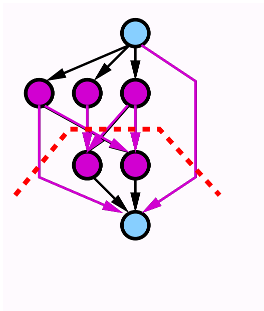

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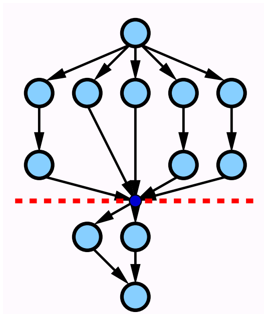

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- It does not keep the layering structure:

  Higher potential overhead even on well-balanced computations

Algorithm 2

- Local resynchronization + Keep layering structure

Theoretical

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Theoretical

- Local resynchronization + Keep layering structure
- Procedure:
  1. Compute depth levels
  2. For each layer top-down
     (a) Detect local NSP problems between nodes in this and previous layer
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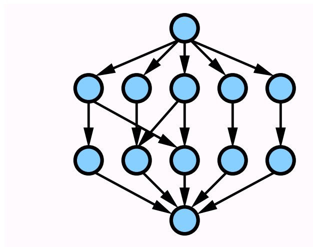

Algorithm 2

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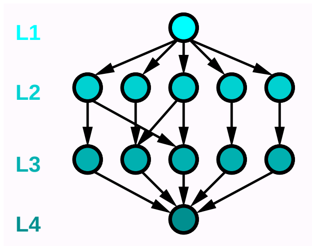

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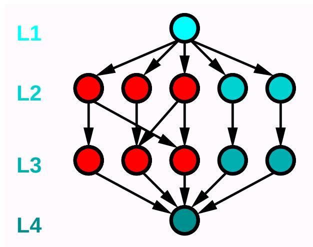

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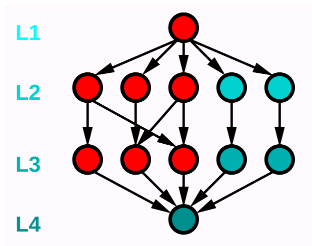

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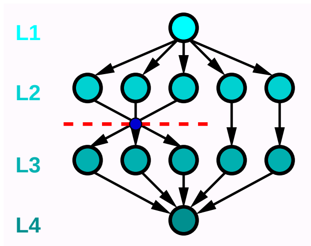

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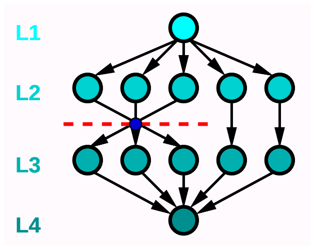

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  Higher complexity than the layering technique
- Similar results as layering for regular NSP structures

  But better results for more irregular, or closer to SP form graphs

Impact indicator

- Objective: Measure the potential performance impact of an SP-ization

  Critical path value (cpv) analysis: Cost model of performance

Theoretical

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- Other structural impact metrics are not related with the potential performance loss [Dissertation 3.6.2]

SP vs. NSP cpv analysis

- Absence of real workload information: Stochastic workloads

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- Further experimental study is needed

  to predict the loss of performance in a generic case

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- Objective:
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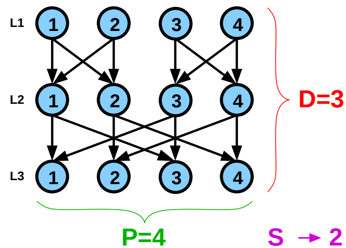

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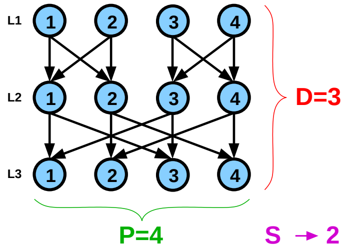

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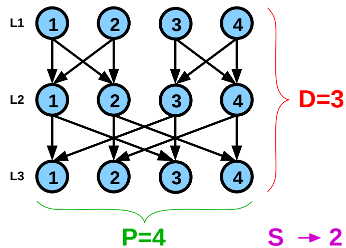

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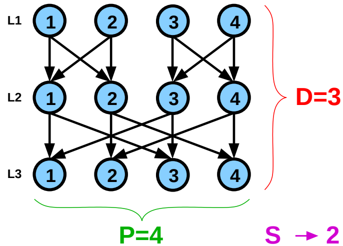

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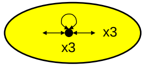
γ levels of detail



Algorithm

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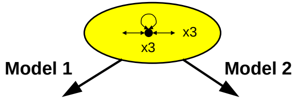

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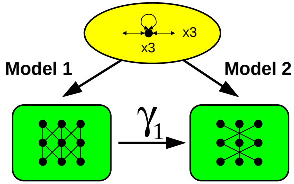

Algorithm

Programming

Experimental

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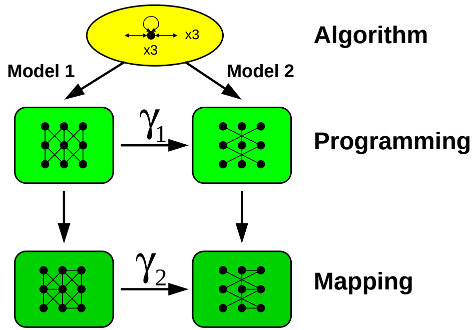

Experimental

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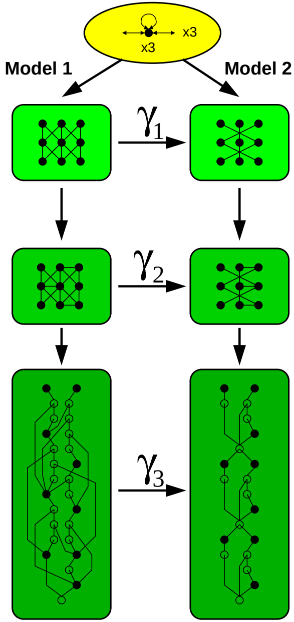

Algorithm

Programming

Mapping

Implementation

γ levels of detail

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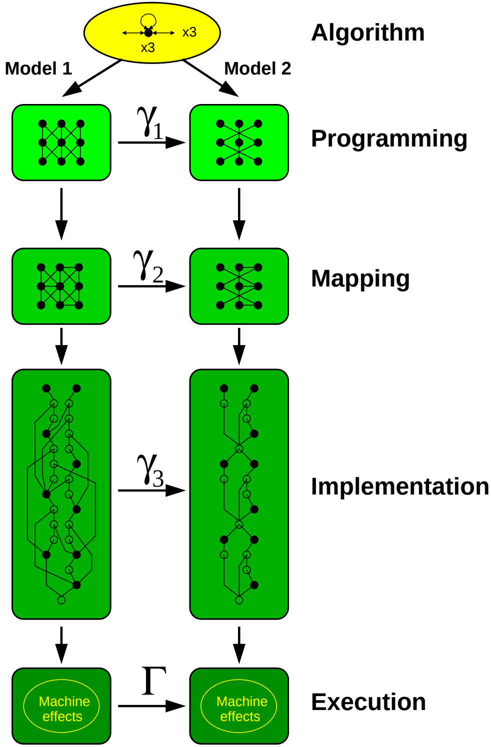

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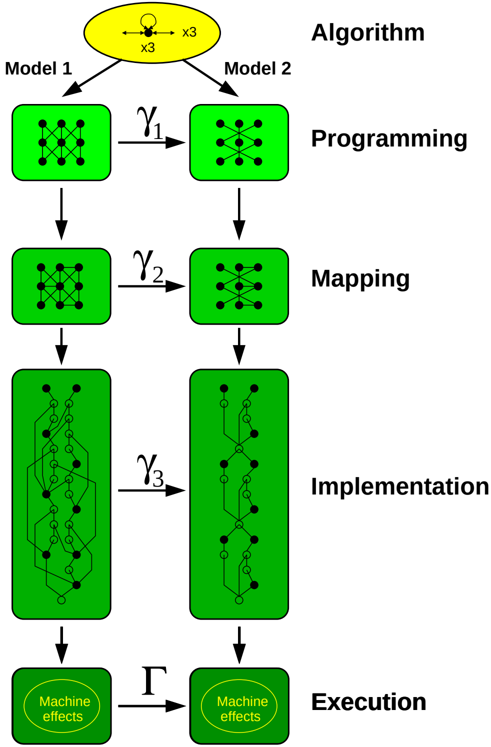

Experiments design - I

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Synthetic graphs

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Experiments design - II

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- Workload: 25 draws for each topology and ς value

Experiments design - III

Real static applications

- Easy graph modeling at any level of detail

Experimental

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  - Execution level: MPI implementations (SP version with barriers)

[Dissertation 4.2.1]

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    [Dissertation 4.2.1]
- Execution level: Three architectures
  - CC-NUMA (Origin2000)
  - Message-passing with low latency (CrayT3E)
  - Distributed memory with high latency (Beowulf)

Experiments design - IV

Experimental

Real dynamic applications

- Two cases:
  1. Structure can be reconstructed from input data structure
  2. Structure can be obtained only by tracing in run-time

Experiments design - IV

Experimental

Real dynamic applications

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- Typically more irregular than static applications
- One example application of each type

- Six real input data examples for each application

Experiments design - V

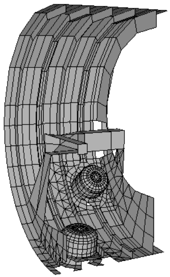
Iterative PDE solver

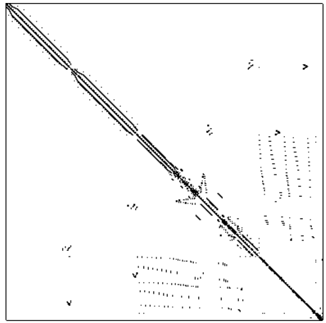
Experiments design - V

Iterative PDE solver

- Six real structural engineering examples

  Matrix Market: Harwell-Boeing, Everstine's collection.





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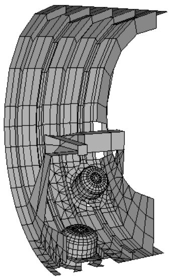

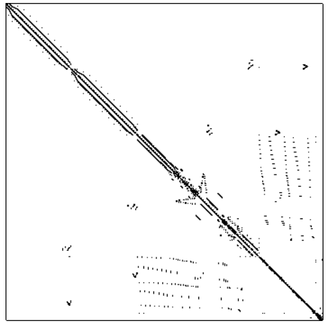

- Sparse matrix data is partitioned for data-layout

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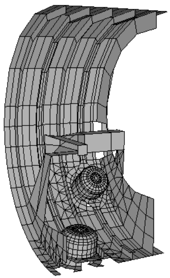

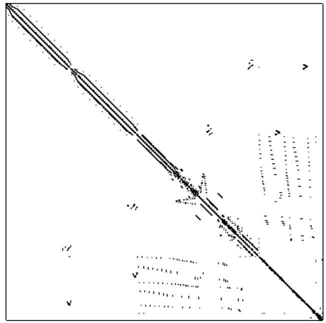

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  State-of-the-art partitioning software: METIS

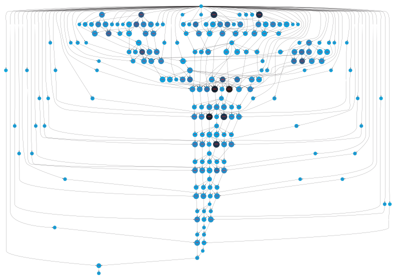
- Mapping level graph reconstructed
- Workload per task estimated as a function of data-layout

Experiments design - VI

Experimental

Domain decomposition and sparse matrix factorization

- Real software oriented to structural engineering: DIANA + Tgex



Experiments design - VI

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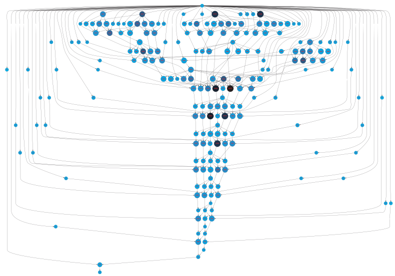

- We use six example mapping level graphs reconstructed from tracing information obtained in a previous work [Lin94,96]

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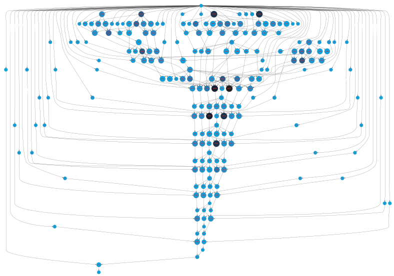

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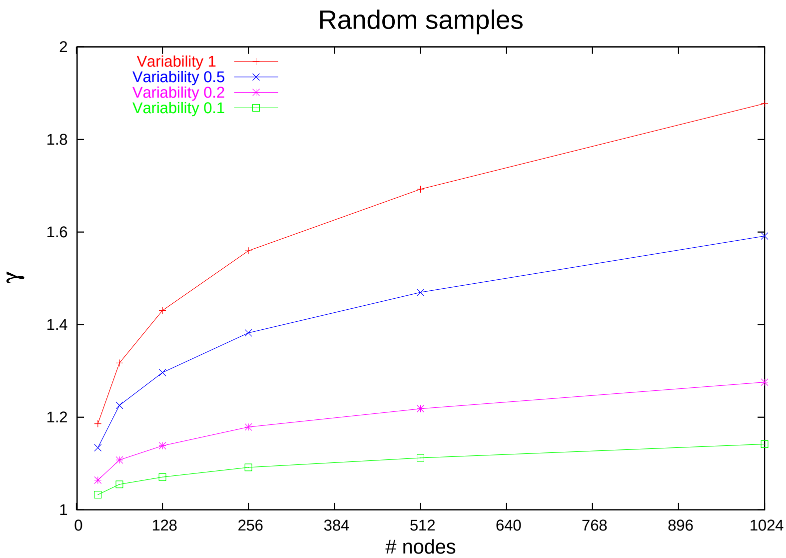
- Real execution workloads provided

Results: Workload

Experimental



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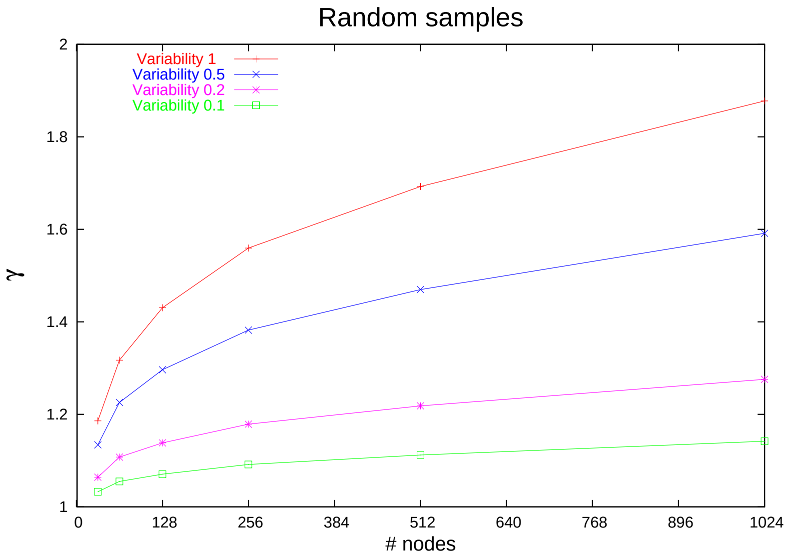

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- High workload unbalance ⟶ Increasing performance loss

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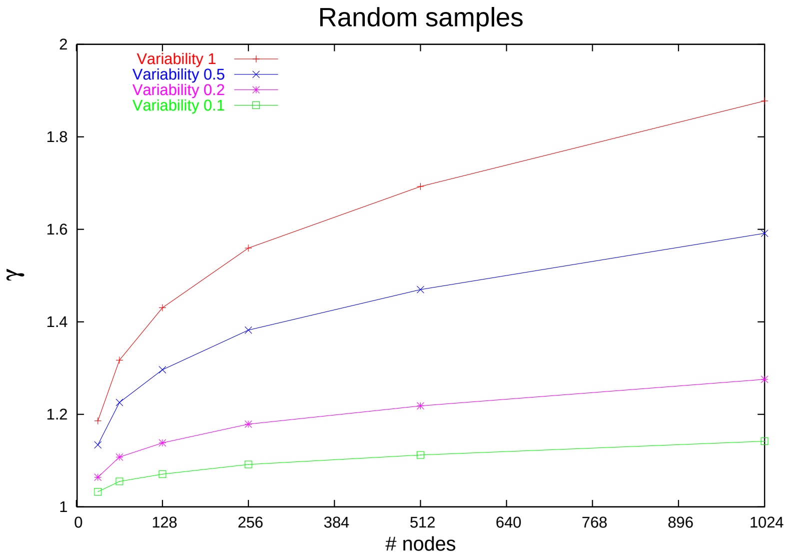

- Low workload unbalance $\longrightarrow$ Minimal performance loss
- High workload unbalance $\longrightarrow$ Increasing performance loss
- Workload correlation with layers or vertical instances of nodes

  Reduced performance loss [Dissertation 4.1.3]

Experimental

Results: Graph size parameters P, D

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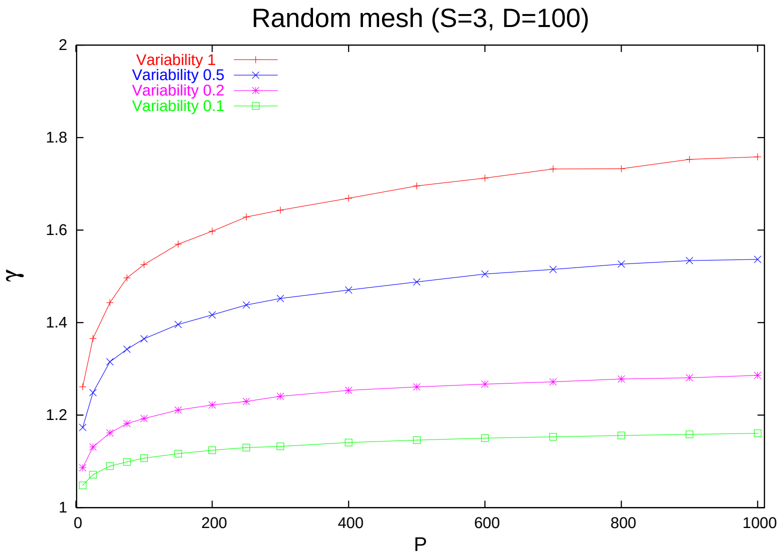

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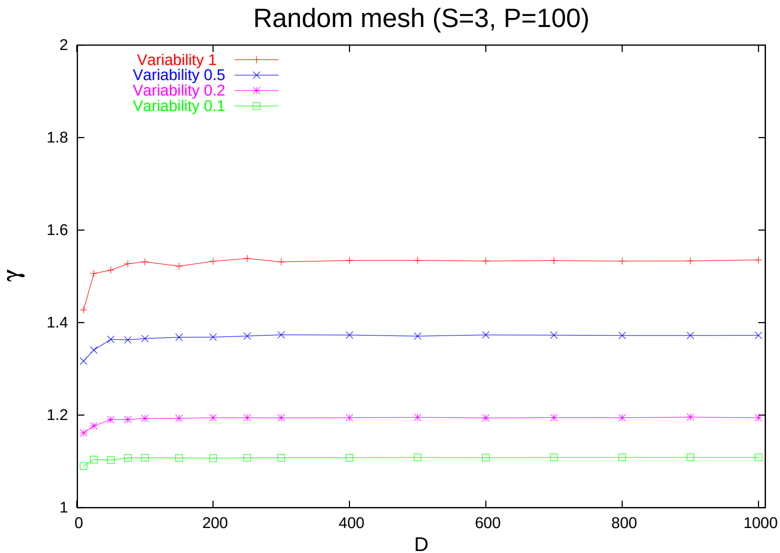

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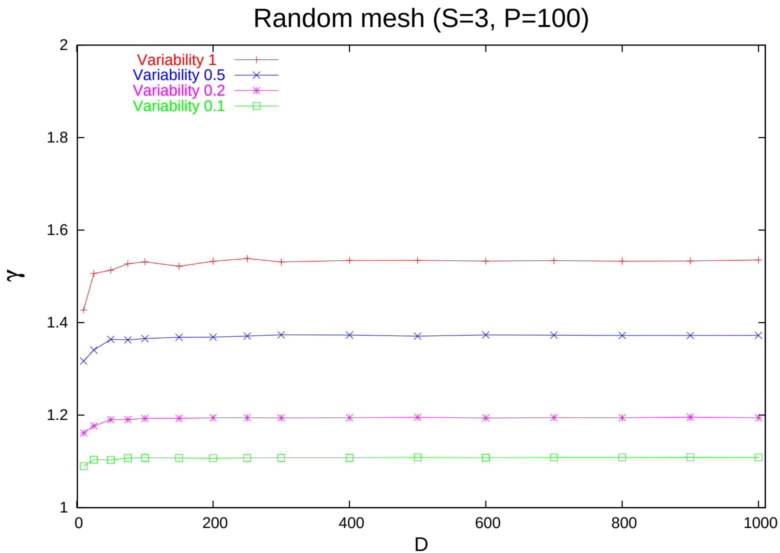

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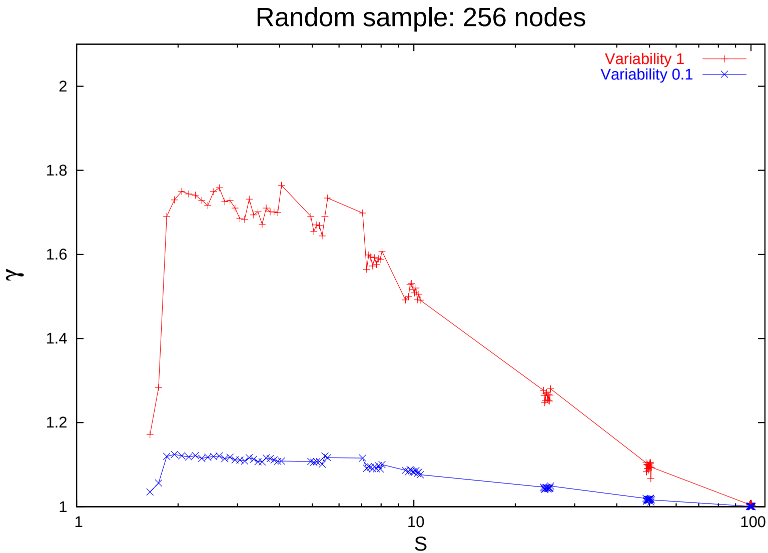
Pathological effects characterization and metric [Dissertation 4.1.3]

Experimental

Results: Graph parameter S



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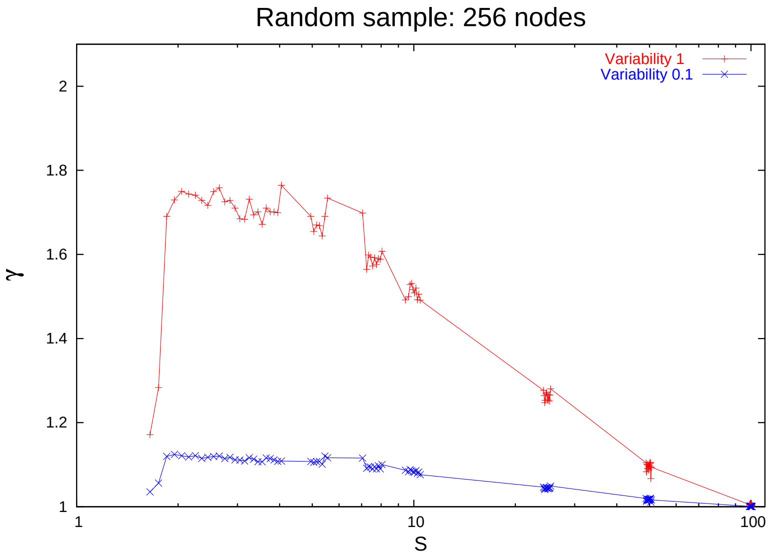
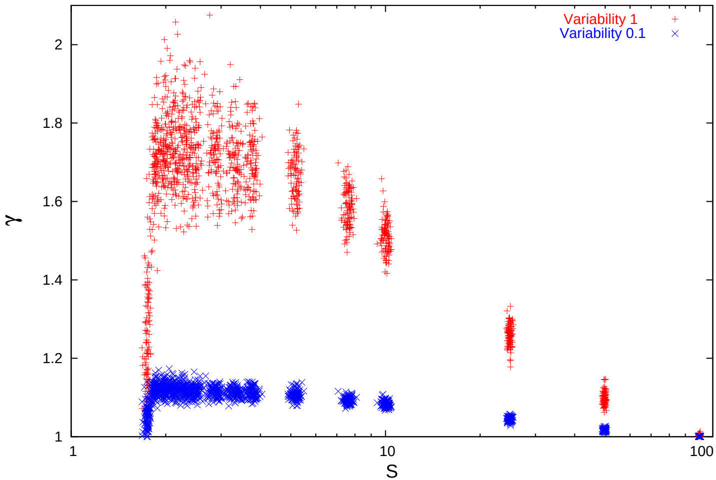


- S increase has opposite effect to P
- $S < 2$ implies sparse graphs containing SP series subgraphs

Results: Graph parameter S

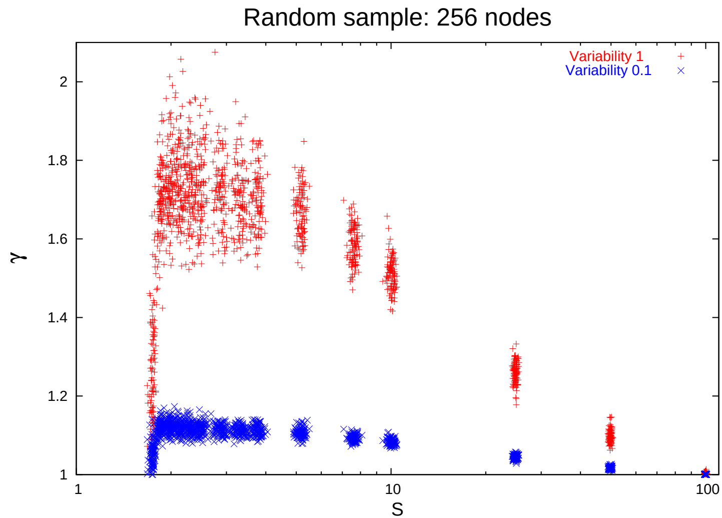
Random sample: 256 nodes



- Maximum dispersion around $S = 2$

Experimental

Results: Graph parameter S



- Maximum dispersion around $S = 2$
- Asymptotic predictions:

$$\overline{\gamma} \approx \frac{\mu + \sigma\sqrt{\log(P)}}{\mu + \sigma\sqrt{\log(S)}}$$

Experimental

Results: Execution level Γ

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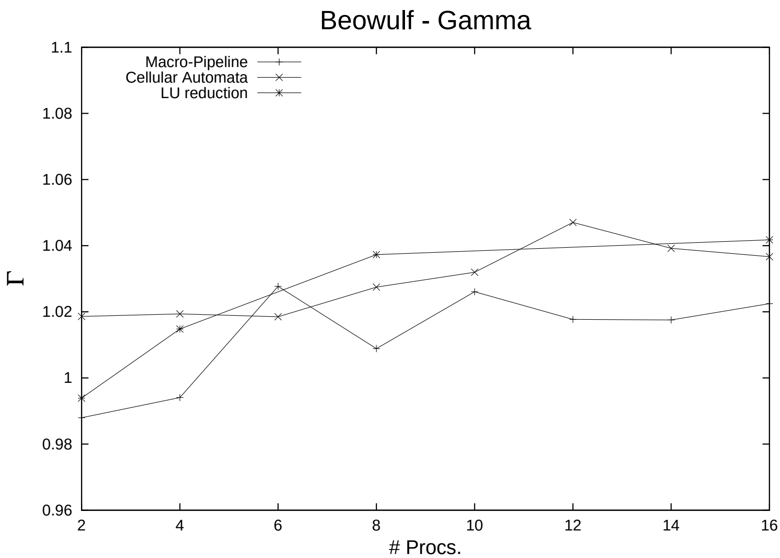

- Static applications: Extremely balanced workloads, negligible γ

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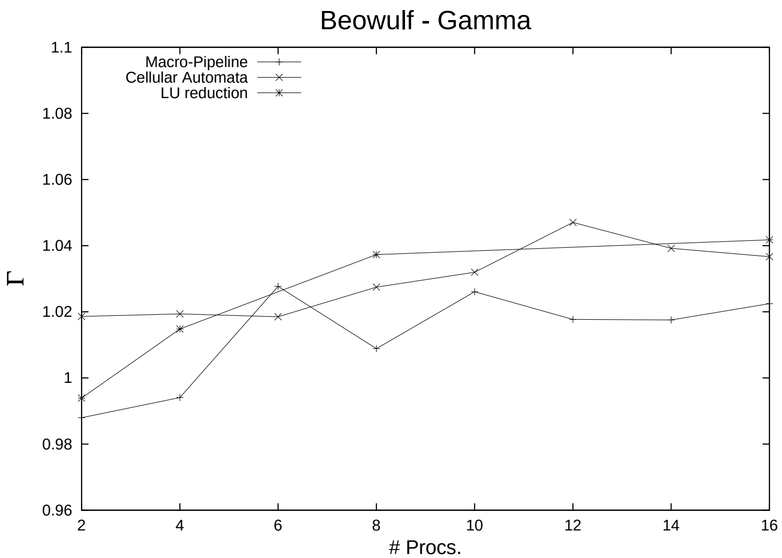

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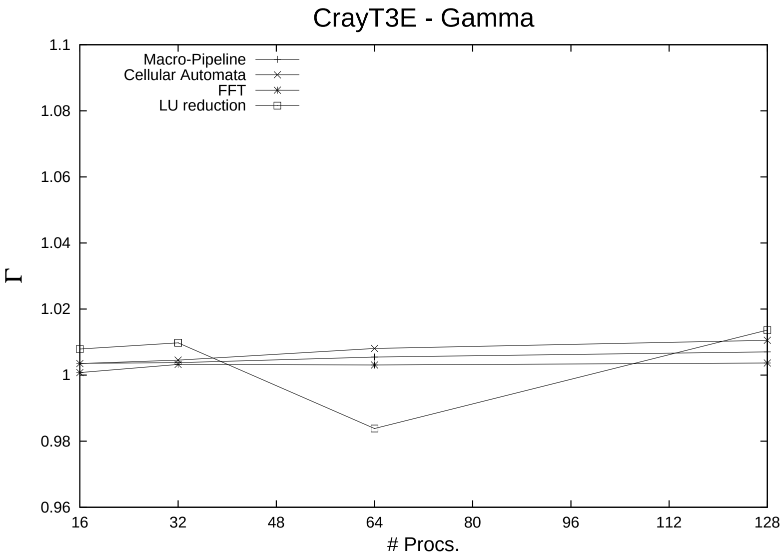

- Static applications: Extremely balanced workloads, negligible γ
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However, sometimes communications perform better in presence of a barrier!

Results: Dynamic applications - I

Sparse iterative solvers

- METIS partitioning produces very well workload and synchronization balance

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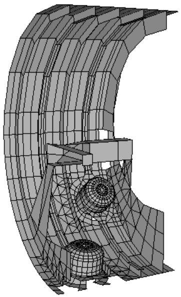

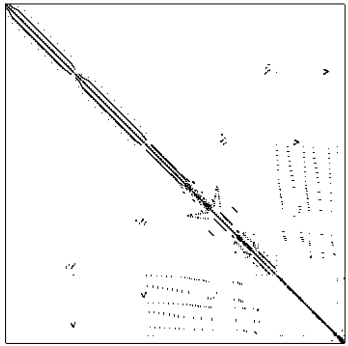

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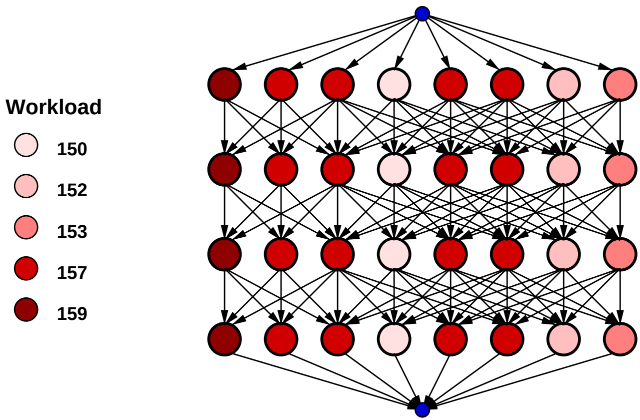

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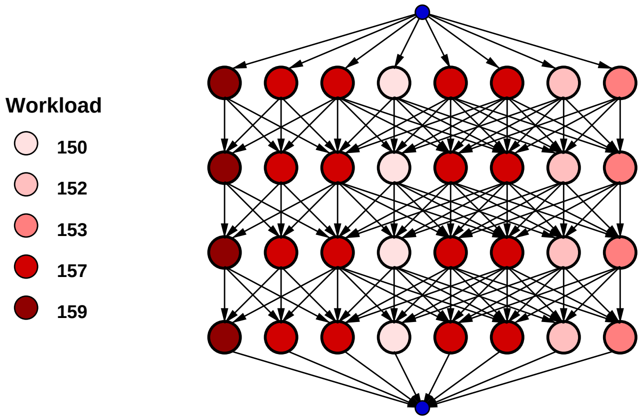

- Negligible loss of performance: Expected for any good load-balancing technique

Results: Dynamic applications - II

Experimental

Domain decomposition and sparse matrix factorization

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- Real workload even lower:

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- Domain decomposition data-layout produces workload and topology regularities

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  SA: Key for the expressive power vs. analyzability trade-off
- The expressive power restriction associated with SP PPMs has been investigated in-depth both theoretically and empirically

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- Methodology: Three-way approach
  - Conceptual: Models and applications review, SA classification.

    Qualitative study

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  - Conceptual: Models and applications review, SA classification.

    Qualitative study

  - Theoretical: SP, NSP graph characterization and algorithmic transformation techniques
  - Experimental: Empirical analysis framework for the potential negative performance impact of SP programming at different levels of detail, including propagation to execution level

Results

- At the design or programming level (γ):
  Correlation between the SP potential loss of parallelism with simple application parameters:
  - $\boldsymbol{P}$ has an under-logarithmic-like effect on $\boldsymbol{\gamma}$
  - $\boldsymbol{S}$ has a positive inverse effect
  - Variability ($\boldsymbol{\varsigma}$) has the major impact on $\boldsymbol{\gamma}$

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  It almost does not scale with the problem size!

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- SP SA is a promising design concept for portable, efficient, easy-to-use and general-purpose PPMs

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- Further experiments with more irregular applications
- New NSP to SP transformations:
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- Real SP programming framework development:

  Automatic mapping and scheduling guided by performance cost analysis

Main contributions

- CPC 2003, Tenth International Workshop on Compilers for Parallel Computers, Amsterdam, The Netherlands
- VecPar 2002, 5th International Meeting, High Performance Computing for Computational Science, Porto, Portugal (Best Student Paper Award)
- CPC 2001, Ninth International Workshop on Compilers for Parallel Computers, Edinburgh, Scotland
- VecPar 2000, 4th International Meeting on Vector and Parallel Processing, Porto, Portugal
- CPC 2000, Eigth International Workshop on Compilers for Parallel Computers, Aussois, France
- Parallel Computing ParCo'99 Delft, The Netherlands
- Euro-PDS'97, IASTED International Conference, Parallel and Distributed Systems, Barcelona
- ASCI'97, Proceedings of the third annual conference of the Advanced School for Computing and Imaging, Heijen

Questions?

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